REMARKS

This is in response to the Office Action dated December 23, 2003, claims 1, 2, 4-18, 20-22 are pending. The Examiner's reconsideration of the rejections is respectfully requested in view of the amendments and remarks.

Claims 1-16 have been rejected under 35 U.S.C. 102(e) as being anticipated by Houston (U.S. Patent No. 6,307,281). The Examiner stated essentially that Houston teaches all the limitations of claims 1-16.

Claims 1 claims, *inter alia*, "a selection device coupled to the at least one logic circuit, the selection device providing switching of on/off states of the at least one logic circuit based on a stored logical value, wherein the selection device includes a switch which provides a connection from ground to a power line of the at least one logic circuit in an on state." Claim 9 claims, *inter alia*, "a selection device coupled to each of the functional groups, each selection device providing switching of on/off states of the corresponding functional group based on logical values stored in a register, wherein the register is coupled to each functional group through a corresponding selection device."

Houston teaches a method for selective allocation of power to elements of a circuit (see Abstract). Houston teaches that an element is controlled by a register connected to a field effect transistor coupled between a source voltage (V_1) and the element (see Figure 4). Houston does not teach, "the selection device includes a switch which provides a connection from ground to a power line of the at least one logic circuit in an on state" as claimed in claim 1. Houston teaches that the element is connected directly to a ground voltage (see Figure 4). Houston does not teach that a selection device includes a switch coupled between a ground voltage and the element. Therefore, Houston fails to teach all the limitations of claim 1.

Referring now to claim 9; Houston teaches that an element is connected to a register through a selection device (see Figure 4 and Figure 5). Houston does not teach "a selection device coupled to each of the functional groups, each selection device providing switching of on/off states of the corresponding functional group based on logical values stored in a register, wherein the register is coupled to each functional group through a corresponding selection device" as claimed in claim 9. Each register of Houston is connected to an individual element. Houston does not teach a register coupled to each functional group. Therefore, Houston fails to teach all the limitations of claim 9.

Claims 2, and 4-8 depend from claim 1. Claims 10-16 depend from claim 9. The dependent claims are believed to be allowable for at least the reasons given for the respective independent claims. At least claims 8, 11 and 16 are believed to be allowable for additional reasons.

Claim 11 claims "the selection devices each include a switch which provides a connection from ground to a power line of the functional group in an on state." Claims 8 and 16 claim, *inter alia*, "an output table including logical states corresponding to power-saving on/off states."

Referring to claim 11; Houston teaches that an element is controlled by a register connected to a field effect transistor coupled between a source voltage (V_1) and the element (see Figure 4). Houston does not teach, "the selection devices each include a switch which provides a connection from ground to a power line of the functional group in an on state" as claimed in claim 11. Houston teaches that the element is connected directly to a ground voltage (see Figure 4). Houston does not teach that a selection device includes a switch coupled between a ground voltage and the element. Therefore, Houston fails to teach all the limitations of claim 11.

Referring to claims 8 and 16; Houston teaches that a logic component inspects instructions in an execution queue in order to determine which elements such instructions shall utilize (see col. 5, lines 54-57). Houston does not teach an output table as claimed in claims 8 and 16. Nowhere does Houston teach how a determination of which elements an instruction will use is handled, much less that an output table includes logical states corresponding to power-saving on/off states. Therefore, Houston does not teach that an output table including logical states corresponding to power-saving on/off states as claimed in claims 8 and 16.

The Examiner's reconsideration of the rejection is respectfully requested.

Claims 17-20 have been rejected under 35 U.S.C. 102(e) as being anticipated by Bartley (U.S. Patent No. 6,219,796). The Examiner stated essentially that Houston teaches all the limitations of claims 17-20.

Claim 17 claims, *inter alia*, "comparing a number of instruction cycles for which each logic circuit will be inactive after a current instruction cycle to a value for each instruction cycle of the functional program, wherein the value of the comparing step includes a number determined to provide net power savings in the logical circuits."

Bartley teaches a method of optimizing a computer program for reduced power consumption by a processor (see Abstract). Bartley teaches that a compiler compares the period of non-use with thresholds of various power modifying instructions (see col. 7, lines 55-61). Bartley does not teach that "the value of the comparing step includes a number determined to provide net power savings in the logical circuits", essentially as claimed in claim 17. Bartley's power modification instructions have thresholds. However, Bartley does not teach that the thresholds consider a net power savings. Therefore, Bartley fails to teach all the limitations of claim 17.

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Claims 18, 20 and 21 depend from claim 17. The dependent claims are believed to be allowable for at least the reasons given for claim 17. At least claim 21 is believed to be allowable for additional reasons.

Claim 21 claims, "wherein the value for each instruction cycle of the function program includes a number of cycles needed to execute an instruction sequence to turn each logical circuit on or off."

Bartley teaches that a compiler compares the period of non-use with thresholds of various power modifying instructions (see col. 7, lines 55-61). Bartley does not teach that "the value of the comparing step includes a number determined to provide net power savings in the logical circuits", essentially as claimed in claim 17. Bartley's power modification instructions have thresholds. However, Bartley does not teach that the thresholds include a number of cycles consumed by the power modification instructions themselves. Therefore, Bartley fails to teach all the limitations of claim 21.

The Examiner's reconsideration of the rejection is respectfully requested.

Accordingly, claims 1, 2, 4-18, 20-22 are believed to be allowable for at least the reasons stated. The Examiner's withdrawal of the rejections is respectfully requested. For the forgoing reasons, the application is believed to be in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

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